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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,936	03/19/2004	Youn-cheul Kim	SAM-0548	8220
7590	05/18/2005		EXAMINER	
Steven M. Mills MILLS & ONELLO LLP Suite 605 Eleven Beacon Street Boston, MA 02108			COX, CASSANDRA F	
			ART UNIT	PAPER NUMBER
			2816	
			DATE MAILED: 05/18/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,936	KIM, YOUN-CHEUL	
Examiner	Art Unit		
Cassandra Cox	2816		

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 19 March 2004.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-5 is/are pending in the application.
4a) Of the above claim(s) 4 and 5 is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-3 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 19 March 2004 is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ .

5) Notice of Informal Patent Application (PTO-152)

6) Other: ____ .

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
 - I. Claims 1-3, drawn to duty cycle correction circuit, classified in class 327, subclass 175.
 - II. Claims 4-5, drawn to delay locked loop, classified in class 327, subclass 156.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions II and I are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the delay locked loop does not require the specific elements recited in the duty cycle correction circuit. The subcombination has separate utility such as a data processor.
3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Stephen Mills on 05/11/05 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-3.

Affirmation of this election must be made by applicant in replying to this Office action.

Claims 4-5 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Shin (U.S. Patent No. 6,342,801).

In reference to claim 1 Shin discloses in Figure 5 a duty cycle correction circuit of a delay locked loop comprising: a differential amplifier (432), which receives and amplifies differential reference clock signals (clk_i, clk_{ib}) through a first input terminal and a second input terminal, and outputs differential output signals to a first differential output terminal and a second differential output terminal, respectively, a first transmission circuit (P9, N19), which is connected between the first differential output terminal and a first node (N16), and transmits a signal of the first differential output terminal to the first node, in response to transmission control signals (caponb, capon), a second transmission circuit (N20, P12), which is connected between the second differential output terminal and a second node (N17), and transmits a signal of the second differential output terminal to the second node, in response to the transmission control signals (caponb, capon), a first storage unit (N23), which is connected between the first node and a ground voltage and accumulates electric charges on the first node;

a second storage unit (N27), which is connected between the second node and the ground voltage and accumulates electric charges on the second node; and a current control circuit (P13, N24, P14, INV9, P15, N28, P16, INV10), which controls an amount of electric charges accumulated in the first storage unit (N23) and an amount of electric charges accumulated in the second storage unit (N27), in response to a corresponding switching control signal (pdn), see specification column 7, lines 5-50 wherein the amount of electric charges accumulated is seen to be proportional to the charging time of each capacitor (N23, N27).

In reference to claim 2 Shin discloses in Figure 5 wherein each of the first transmission circuit (P9, N19) and the second transmission circuit (N20, P12) is a transmission gate.

In reference to claim 2 Shin discloses in Figure 5 wherein each of the first storage unit (N23) and the second storage unit (N27) is a MOS transistor.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC
Cc
May 14, 2005



TUANT. LAM
PRIMARY EXAMINER